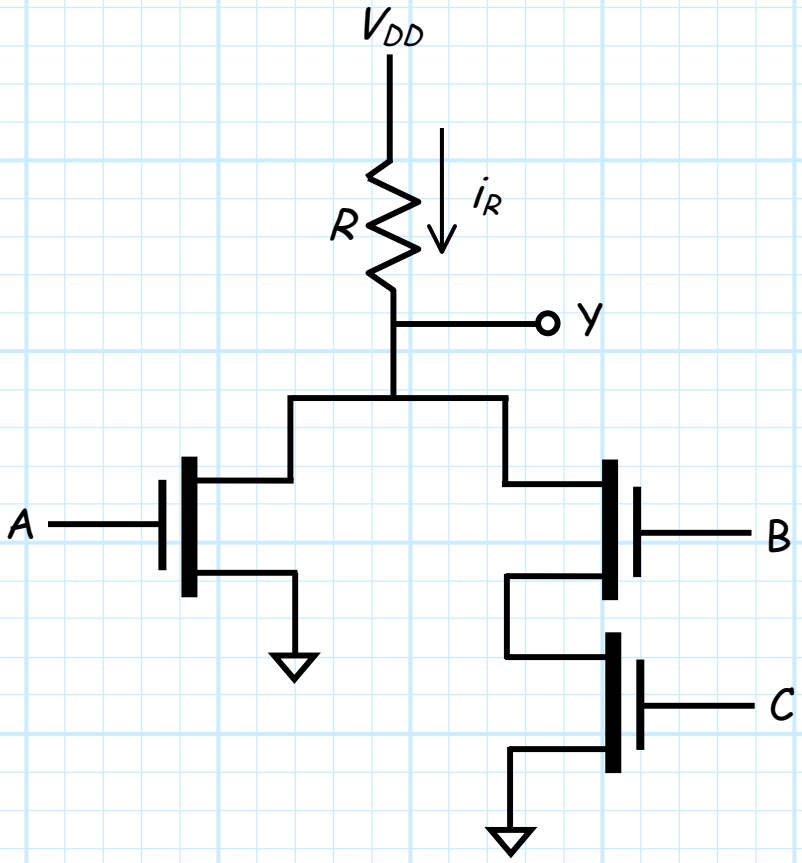
NMOS Logic Circuits

An alternative way to construct a digital logic gate is to simply use a single **large resistor** as the pull-up network!



If the PDN is **open**, no current will flow (i_R =0), and thus there will be **no** voltage drop across the **Pull-Up Resistor** *R*—the output will be high, **just** like before!

But, if the PDN **is** conducting, current **will** flow ($i_R \neq 0$), and thus there **will** be a large voltage drop across *R*—the output will be **low** (sort of)!

This method of constructing digital devices is called **NMOS logic** (for hopefully **obvious** reasons!).

Q: *Why would we want use NMOS logic?*

A: Replacing the PUN with a single resistor greatly **simplifies** and **shrinks** the circuit. For complex gates (i.e., gates with **many** inputs), we can reduce the number of required devices (transistors and resistors) by **nearly half**!

Q: *Yikes! This seems to be **a lot** better. Why wouldn't we **always** use NMOS logic?*

A: There are **two** really big problems with NMOS logic (at least, when compared to **CMOS**):

1. Since current flows when the output is low, the static power dissipation is **not zero**.

2. Since current flows when the output is low, V_{OL} is **not** equal to its ideal value of **zero** (i.e., $V_{OL} \neq 0$)!

Additionally, there is **one more** problem when implementing NMOS in **integrated circuits**. IC resistors are (relatively) very large and difficult to construct.

→ This problem, though, is easily solved—we replace the **pull-up resistor** with an **active load**.